

DESIGN DOCUMENT

Client - Professor Alexander Stoytchev

Team 31 - Curriculum for the i281e

Team Members Ethan Uhrich - Team Lead & Treasurer Ariana Dirksen - Editor & Note Taker Tessa Morgan - Task Manager & Webmaster Gigi Harrabi - Client Interaction & Outreach Coordinator

> Contact - sdmay25-31@iastate.edu Website - <u>https://sdmay25-31.sd.ece.iastate.edu/</u> Revised: 12/6/2024 V1

Executive Summary

Our project aims to create a series of labs to act as a curriculum for undergraduate engineering students. The goal of these labs is to introduce students to digital circuits and microprocessors. They are expected to bridge the gap between embedded systems, electronic circuits and digital logic. This will help students better understand how the logic is implemented in hardware and how the software interacts with the hardware. Our design must support hardware focused labs, software focused labs and labs that tie both together. Our design will create reusable testing circuits and programs to allow students to verify their work on the labs. Furthermore, our design must allow students to complete the labs within three hours. With these considerations in mind we focus on hardware labs first then transition to labs that tie software into the hardware and wrap up with software focused labs. Throughout the labs students will use breadboards, microchips, circuit components such as resistors, LEDs, capacitors and wires, ribbon cables and EEPROM memory to implement the various components in the hardware labs. For the software labs students will utilize the EEPROM memory and the i281 simulator to visualize their programs and complete software labs. As these labs build on each other through implementing components of the i281e processor, students can visualize how the various components in the processor work together. So far, we have created four labs, have concepts and basic designs for an additional seven and concepts for two projects for students to complete. Of our created labs two have been thoroughly tested and can be completed in an hour. Additionally, after testing another was found to be too time consuming to be a standalone lab and was broken down into two labs. As much of our testing is reliant on the time it takes to complete the labs and user experience going through the lab we need to test the labs with a focus group. Alongside that we need to finish creating the rest of our labs and iron out more details for the projects. Lastly, we also plan to build at least one additional PCB implementation of the CPU and will ideally also create one to two outreach activities at the middle and high school level.

Learning Summary

Development Standards & Practices Used

For standard circuit practices we maintained implementation standardization across our hardware and followed a uniform procedure in our documentation and lab manuals. We also use the following engineering standards for this project.

- IEEE 610.10-1994
- IEEE 610.13-1993
- IEEE 1515-2000

Summary of Requirements

- Undergraduate students must be able to complete labs in three hours.
- Labs must be at an appropriate level of difficulty for undergraduate students.
- Lab instructions must clearly communicate all information needed to complete the lab.
- Hardware lab implementations of the i281e components must remain compatible with the PCB implementation.
- Labs must be easy for the students to test and verify the accuracy of their implementations.

Applicable Courses from Iowa State University Curriculum

Courses
EE 201: Electric Circuits
EE 230: Electronic Circuits and Systems
CprE 281: Digital Logic
CprE 288: Embedded Systems
CprE 381: Computer Organization and Assembly Level Programming

Table 1 - Applicable courses for the Curriculum for the i281e Processor project

Acquired Skills

The team has learned many new skills while working on designing and implementing our project. Members of the team have learned how to enforce standardization practices, draw schematics in KiCad and create simulations in TinkerCAD.

Table of Contents

1. Introduction	8
1.1. Problem Statement	8
1.2. Intended Users	8
2. Requirements, Constraints, And Standards	9
2.1. Requirements & Constraints	9
2.1.1. Physical Requirements	9
2.1.2. Functional Requirements	9
2.1.3. Resource Requirements	9
2.1.4. Requirements for Outreach Events	10
2.1.5. Additional Requirements and Constraints	10
2.2. Engineering Standards	11
3. Project Plan	12
3.1. Project Management/Tracking Procedures	12
3.2. Task Decomposition	12
3.3. Project Proposed Milestones, Metrics, and Evaluation Criteria	12
3.4. Project Timeline/Schedule	13
3.5. Risks and Risk Management/Mitigation	14
3.6. Personnel Effort Requirements	15
3.7. Other Resource Requirements	16
4. Design	17
4.1. Design Context	17
4.1.1. Broader Context	17
4.1.2. Prior Work/Solutions	18
4.1.3. Technical Complexity	18
4.2. Design Exploration	19
4.2.1. Design Decisions	19
4.2.2. Ideation	19
4.2.3. Decision-Making and Trade-Off	19
4.3. Proposed Design	20
4.3.1. Overview	20
4.3.2. Detailed Design and Visuals	20
4.3.3. Functionality	20

4.3.4. Areas of Concern and Development	21
4.4. Technology Considerations	21
4.5. Design Analysis	22
5. Testing	23
5.1. Unit Testing	23
5.2. Interface Testing	24
5.3. Integration Testing	24
5.4. System Testing	24
5.5. Regression Testing	24
5.6. Acceptance Testing	24
5.7. Results	24
6. Implementation	26
6.1. Implementation Process	26
6.2. Drafting Labs	27
6.3. Current Progress	28
7. Ethics and Professional Responsibility	31
7.1. Areas of Professional Responsibility/Codes of Ethics	31
7.2. Four Principles	32
7.3. Virtues	33
8. Closing Material	35
8.1. Conclusion	35
8.2. References	36
8.3. Appendices	37
8.3.1. Research	37
9. Team	39
9.1. Team Members	39
9.2. Required Skill Sets for Your Project	39
9.3. Skill Sets covered by the Team	40
9.4. Project Management Style Adopted by the team	40
9.5. Initial Project Management Roles	40
9.6. Team Contract	41

List of Tables

Table 1 - Applicable courses for the Curriculum for the i281e Processor project	3
Table 2 - Resource Requirements.	10
Table 3 - Personal Effort Requirements by Task Breakdown	15
Table 4 - Design Considerations	18
Table 5 - Professional Area of Responsibility	31
Table 6 - Four Principles	32
Table 7 - Virtues and Improvements within the Team	34
Table 8 - Product Research	38
Table 9 - Skills Needed for the Project	39
Table 10 - Skills Covered by the Team	40

List of Figures

Figure 1 - Gantt Chart	14
Figure 2 - Breadboard Mockup of Test board Connected to PC Circuit	23
Figure 3 - Initial Implementation Lab 3's 2-to-1 8-bit Bus Multiplexer	26
Figure 4 - Beginning of Lab Manual Template	27
Figure 5 - First Section of Lab 1 Report Template	28
Figure 6 - Excerpt from Lab 3 Manual	29
Figure 7 - Lab 5 & 6 Implementation	30
Figure 8 - Beginning of Lab 7 Implementation	30

1. Introduction

1.1. PROBLEM STATEMENT

The goal of this project is to use open-source hardware and software designs for the existing central processing unit (CPU), operating system (OS), and simulator to implement a set of lab and outreach activities around the i281e processor. The i218e is a processor built completely on the basic logic that makes processors operate. This processor is a minimalistic design intended specifically as a teaching tool for the department.

These labs and activities will help students who have not used the processor adapt to and learn about how to create and work with processors like i281e. Each activity will be an appropriate complexity such that it can be completed by an average undergraduate student in a reasonable amount of time. Each must be tested by the team and documented with detailed step-by-step documentation. For some tasks, video tutorials could be used as well.

The results will be used to support and enhance the curriculum in Computer Engineering and Electrical Engineering. These documents could also be used as educational materials for existing classes or to support future lectures and labs. A subset of these materials will be used for outreach activities to get the next generation of engineers excited about computers. Part of this project is also to acquire parts for, assemble, and test several new i281e machines. This process must also be documented to aid students and teaching assistants in building these machines for future use as well as potential hobbyists.

1.2. INTENDED USERS

Our project's main users are students who are interested in embedded systems, but who are either in middle/high school or undergraduates in college. Our second type of users are the TAs who may need the materials (lab documents and equipment) who need to conduct the lab or activity to the students. Our final user is the professor who will have a finalized version of this course that will bridge the gap between digital logic, embedded systems, and computer architecture.

Our users' needs are different for each user. For example, the students need to understand simpler concepts of digital logic and embedded systems so that they can understand what is going on in the lab that they are executing. The needs for TA's are a well-written lab document, a rough outline of the answer key and instructions for how to debug once a student is stuck. The professor's need is for the activities to fill in the knowledge gaps that students must succeed in future courses.

2. Requirements, Constraints, And Standards

2.1. REQUIREMENTS & CONSTRAINTS

Our requirements include physical, functional, and resource requirements.

2.1.1. Physical Requirements

Our team needs to create at least 10 interactive lab-based activities for the students engaging in the lab events. The labs consist of breadboards, wires, buses, chips and LEDs which are sourced from ETG. As well as software, which is free to use, or custom made for the Labs.

2.1.2. Functional Requirements

The labs need to be within the 2- to 3-hour time limit and feasible for undergraduate students to complete.

2.1.3. Resource Requirements

Req. #	Description				
	Lab 1				
1	CD74HC08E Chip				
2	CD74HC32E Chip				
3	CD74HC04E Chip				
4	830-pin Breadboard				
5	Red LED				
6	1.0 kΩ resistor x4				
7	Breadboard Wires				
	Lab 3				
8	830-point Breadboard				
9	Quad 2-1 MUX (SN74HCT257N) Chip x2				
10	0.1 uF Ceramic Capacitor x2				
11	830-pin Breadboard				
12	5mm Yellow LED				
13	330Ω THT Resistor				

r					
14	Breadboard Wires				
15	Flat Cable Plug x3				
16	Connector Wires				
	Lab 5 & 6				
17	CD74HCT283E Chips x4 (Adders)				
18	SN74HCT257N Chips x2 (MUXs)				
19	SN74HCT273N Chip (Register)				
20	830-pin Breadboards x3				
21	Red LED				
22	Green LEDs x7				
23	Yellow LED x2				
24	0.1 uF Capacitor x7				
25	330 Ω resistor x10				
26	Flat Cable Plug x2				
27	Connector Wires				
Additional Resources					
28	i281 + i281e Manuals				
29	Previous Senior Design Team's Documentation				
30	Additional Hardware Components for Future Labs				
31	Any Software required for Software Labs				

Table 2 - Resource Requirements.

2.1.4. Requirements for Outreach Events

Set up educational events by contacting WiSE, middle schools and high schools in our area. Activities need to be achievable for the participants. Resources required must be prepared in advance.

2.1.5. Additional Requirements and Constraints

Our constraints may affect the users since the resources are limited to ETG and what is provided from DigiKey hardware wise. Software wise, all students are required to use free software that may not have

a wide variety of resources. For quantitative and qualitative requirements, our advisor and TAs of CPRE 371x should grade the labs out of 100 points. Students should successfully complete about at least 80% of the prelab and understand the big picture of the lab so they can be capable of relating the lab material to class material. Students should be able to complete the lab within 3 hours, and anything beyond that may inquire for help from the TAs. With the help of the instructor who is responsible for carrying out the training of the TAs, while TAs are expected to guide the student, the TAs should not give away the answers verbatim or assist a student in committing academic dishonesty. They are required to report any kind of plagiarism and cheating.

2.2. ENGINEERING STANDARDS

Engineering standards are important since some, if not most, engineering products depend on the quality of the user's life. While browsing the IEEE Standards website, there are products that are related to healthcare and life sciences that if they do not follow the IEEE standards and other codes, will affect the user's life negatively.

IEEE Standard Glossary of Hardware Terminology (IEEE 610.10-1994)- Describes official definitions related to computer hardware relating to computer architecture, computing storage, processors and components [5].

IEEE Standard Glossary of Computer Languages (IEEE 610.13-1993)- Describes the names and definitions of computer languages, and their historical significance [6].

IEEE Recommended Practice for Electronic Power Subsystems: Parameter Definitions, Test Conditions, and Test Methods (IEEE 1515-2000)- Describes testing methods for electronic circuits and systems [4].

The first standard relates to the specific terms that will be used in the i281e processor from an educational perspective. Meaning that those terms will be used to describe and teach the participants during the lab activities. The second one is also relevant because in later labs, we will incorporate the use of a computer language on the operating system, for example, and the use of that standard is important. The third one is important because our project involves building breadboard circuits and testing them

Our team agrees on these standards. These are the main three that will apply to our project as the project is intended for internal use within the department rather than commercial use. Additionally, the project is based around a custom design and just needs to fit the CPU, course curriculum, and faculty constraints.

The modifications we intend to make to abide with the IEEE standards are going to be included within the manual and labs. For example, our team can elaborate on the computing and circuit definitions. In addition, we will ensure that IEEE standards for terminology are used in early labs to familiarize students and others with the terminology that will be used throughout all the upcoming labs.

3. Project Plan

3.1. PROJECT MANAGEMENT/TRACKING PROCEDURES

Our team employs Agile for our project management style as we are working on at least ten separate labs that will effectively work as our milestones. We work out the requirements for each lab with our client, Professor Stoytchev, then design the software or circuits, order parts, build, test, and document the process. From there, we develop the first lab assignment draft which we present to the client. Our client gives us feedback, mainly including changes to lab flow and diagrams and additions to the pre-lab and background sections. We then repeat the drafting and feedback iterations until the client checks off on the final draft. Lastly, we have students (outside the project) run through the lab to ensure it can be completed reasonably and flag any last points of concern.

For this project, we mainly communicate and track everyday progress through Discord as well as via weekly stand-ups. Additionally, we will track our task management in GitLab for the design and research of heavier labs. The labs that require developing software will be tracked in GitLab and will rely heavily on Git.

3.2. TASK DECOMPOSITION

Due to the nature of our project, the task decomposition is very natural. Broadly, we will have ten separate milestones for each finalized lab. We will order parts, build circuits, write a program, test, and document each lab. Some labs, mainly the later ones, will require more design and a research phase. An example of one such lab is the EPROM labs, as our team has yet to gain experience programming or using EEPROMs. These labs will require research to successfully learn the necessary software, such as XGpro, the programmer software. We will also be writing a program to play rock, paper, scissors on the i281 CPU which will be written in assembly and will require familiarity with the custom assembly commands and the memory and writing limitations of the i281 machine.

3.3. PROJECT PROPOSED MILESTONES, METRICS, AND EVALUATION CRITERIA

As stated, we have ten clearly defined milestones in the form of completed lab manuals. We will keep track of the time it took us to build the circuits or write the final code for each lab. Using that knowledge, we will tailor each lab to be completed within a 2- to 3-hour lab by undergraduate students, predominantly in their sophomore and junior years. To accurately measure this, we will test our drafted manuals on students to verify they can be completed in an appropriate amount of time. Within some of the more hardware-focused labs, we are also testing our implementations thoroughly to ensure that the logic works the way it is designed to.

Our main evaluation criteria and metrics are based on feedback from students that complete the final labs. We will create a worksheet for students to complete before and after working on the lab to judge this. During the semester, we will have students (who have completed CprE 2810 and are not in senior design) run through completed lab assignments and gather this feedback.

3.4. PROJECT TIMELINE/SCHEDULE

September-October (red): We researched the i281 processor by looking at past documents and lectures provided by our advisors and previous i281e groups.

October-November (pink): Our team built two copies of the MUX, in groups of two since the labs and outreach events are going to be completed in groups of two, tested the MUX and gone through multiple iterations of the documentation process.

November-February (Orange): Our team built two versions of the program counter which have been tested. They require a clock for the register, so we added a debouncer to the testing circuit to accomplish that. The initial materials for the first draft are also created including several diagrams and the visuals for the activity section of the lab. This lab has also been divided into two parts since we started working on it. Going forward, we're going to add to this lab to include hardware debugging activities.

November-December (Yellow): We put together the introduction lab which will walk students through building a 2-to-1 multiplexor which will lead into later labs. This lab has also gone through multiple stages of documentation and is nearly finalized.

December-January (Green): We started the EEPROM lab which includes programming an EEPROM to store the addresses for a 7-segment decoder. We have built the circuit for this and attempted programming the EEPROM and are currently in the testing stages of this lab.

January-February (Light Green): This lab is going to focus on debouncing techniques, basic hardware components such as LEDs and resistors, and reading datasheets.

February-April (Turquoise): This lab will be an introduction to schematics and using KiCAD. We plan to work on this lab during lighter loads throughout the semester which is why it is split in two. This lab will overlap with a mini project in which students build and order parts to make a bus mux on a PCB.

February-March (Blue): This lab will require students to build a clock circuit and will focus on real-time programming and registers.

February-March (Purple): Lab 11 will introduce students to assembly level programming. For this lab we will likely develop a basic program and give students a skeleton code with various challenges to teach them the various commands available with the i281 CPU.

March-April (Lilac): This lab will implement a video game to tie various components of the CPU and previous labs together. The video game will likely be an implementation of rock, paper, scissors using LEDs and 7-segment displays to show the countdown and scores of the game with push buttons as the input.

March-April (Maroon): The peripherals lab exposes students to hooking up peripherals such as joysticks, a printer, a console, or sound output.

April-May (Red and Gray): This final run of the semester will include work on an example final project and building an additional i281 CPU. We have yet to establish the final project, but it may include modifying the ALU, creating another video game, or letting students choose. Even for the open-ended option, we will come up with an example project to tie the rest of our work together and give students something to go from.

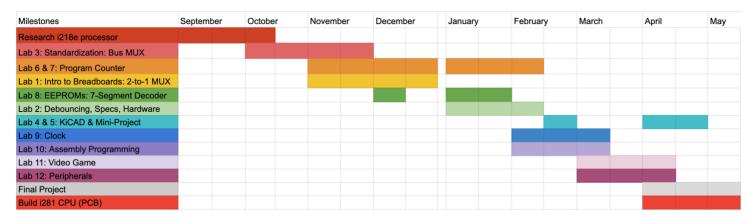


Figure 1 - Gantt Chart

3.5. RISKS AND RISK MANAGEMENT/MITIGATION

The most significant risk for our project is that we cannot order the parts we designed for our hardware implementations. The risk factor is relatively high, as we already dealt with this when ordering our first batch of parts. Thus, if this happens again, we will substitute appropriate replacement parts.

Additionally, our project has a risk that our implementation may not work as expected during testing. In this case, we may have to design alternate implementations and restart our progress in a lab. If this happens with a complicated lab, we plan on scrapping unfeasible labs. This may also require us to create new labs not currently included in our project to replace scrapped ones.

The other risk is that the curriculum committee will not approve this course, and our work will not be used. There is little our group can do outside of ensuring we meet department standards and follow the rules set by ETG to ensure the course is picked up. In the meantime, we must focus on making our project as comprehensive as possible and worthwhile as our capstone projects.

3.6. PERSONNEL EFFORT REQUIREMENTS

Our Labs are created in four stages. First, we design the lab. Then, we implement it using hardware, software, or both. Then, we test any hardware implementations or programs. Then, we document the expected process for the students. Through the course of creating these labs the labs increase in complexity. Some labs, such as Lab 4, require additional research for us to design and implement. Others, like Labs 5 & 6, need more time for documentation as the processes described in the labs are more time-consuming.

Below is a table with the time each lab has taken or is estimated to take. The times listed are cumulative across all members of the team. The design section includes gathering requirements for the overall lab, creating parts lists, ordering components, and deciding on circuit layouts. Implementation consists of building circuits, writing code, and programming components with various software, including later reworking after receiving feedback on previous deployments. Testing consists of all stages of testing circuits, individual components, final testing on students, and gathering feedback from the client. Documentation includes documenting the overall process, assembling lab drafts, generating diagrams/visuals, and taking pictures. This will cover multiple drafts and stages of edit.

Task	Design	Implementation	Testing	Documentation
Lab 1: Intro: MUX	30 minutes	30 minutes	15 minutes	4 hours
Lab 2: Debouncing and Hardware	-		30 minutes	1 hour
Lab 3: Bus MUX	1 hour	3 hours	1 hour	8 hours
Lab 4: Intro to KiCAD	1 hour	3 hours	1 hour	6 hours
Lab 6 & 7: Program 2 hours Counter		6 hours	9 hours	12 hours
Lab 8: EEPROM 30 minutes Programming		2 hours	2 Hours	6 hours
Lab 9: Clock	1.5 hours	5 hours	3 hours	10+ hours
Lab 10: Assembly	2 hours	6 hours	4 hours	10+ hours
Lab 11: Video Game	3 hours	10+ hours	4 hours	10+ hours
Lab 12: Peripherals	2 hours	10 hours	6 hours	10+ hours
Final Project	3 hours	10 hours	6 hours	15+ hours
Test Circuit	30 minutes	3 hours	4 hours	1 hour

Table 3 - Personal Effort Requirements by Task Breakdown

3.7. OTHER RESOURCE REQUIREMENTS

Each lab requires a set component list to complete. The main components we need for our hardwareoriented labs include

- Breadboards
- Assorted Resistors
- Assorted LEDs
- Assorted Wires
- 0.1 uF Ceramic Capacitors
- CD74HCT283E Chips
- SN74HCT273N Chips
- CD74HCT86E Chips
- CD74HCT377E Chips
- CD4078BE Chips
- Ribbon Cable
- EEPROM Programmable Chip
- SRAM Memory

When completing labs, we will also utilize existing materials from the previously compiled GitHub repository containing PCB schematics for each CPU component. We may also reference the physical breadboard implementation to review circuit layouts. In the future, we will also utilize the online simulator for testing.

4. Design

4.1. DESIGN CONTEXT

4.1.1. Broader Context

Our team is tasked to take open-source software and implement them into labs. Students who are at around the sophomore or junior level at Iowa State University are the main users who would benefit from the labs. In addition, anyone who may be interested in our software can replicate our labs, with the list of parts provided in our lab reports and step by step instructions. The professor(s) and TAs teaching the CPRE 371x course and outreach coordinators will also benefit from this since they will be provided with the material and the answer keys.

Area	Description	Examples
Public health, safety, and welfare	Our stakeholders who are the TAs, professors, and outreach coordinators would likely be concerned about the tools and improvement of teaching effectiveness. For students, the project leads to improved learning outcomes through more engaging and effective teaching methods, as well as increased access to academic resources. This creates a more supportive learning environment that fosters student success.	Students will understand and build the knowledge gap between embedded systems (software and hardware) and computer architecture, which includes a range of basic digital logic to more complex components in a RISC-V processor.
Global, cultural, and social	Our project, a community-based engineering education program, reflects the values and aspirations of the local cultural group by prioritizing community engagement and representation. By involving professors, TAs and receiving feedback from students in the planning process, we ensure that the program aligns with the community's emphasis on education as a means of empowerment. Additionally, by recruiting mentors from similar cultural backgrounds, we provide relatable role models who inspire students to pursue careers in engineering fields, ultimately fostering a sense of pride and ownership within the community.	Students and other interested participants will be capable of accessing our open-source software and replicating the labs to further understand our course.
Environmental	One issue may be the concern of wasting wire connections in electrical kits since they are too short or long. A way to combat this is to customize and cut specific wires with certain measurements.	This method would decrease the use of plastic and decrease disposing unneeded wires.

Feenemie	Our project is at low cost. A singular	Our recourses that are provided are at
Economic	Our project is at low cost. A singular	Our resources that are provided are at
	electrical lab kit costs at least about \$15.	relatively low cost to make those labs
	But, at outreach events, students can	but are at no cost to participants who
	participate at no cost.	are willing to learn about the labs.
		Individuals who come across our
		open-source software will need to
		provide their own lab kit. In addition,
		university students who register to
		attend CPRE 371x will be provided
		with a prepared lab kit by the
		university.

Table 4 - Design Considerations

4.1.2. Prior Work/Solutions

Past teams have worked on the i281 CPU. The teams worked on breadboard implementations [8][10], a simulator implementation [9] and a PCB implementation [8]. The gap our team is filling in is an educational implementation, which is a combination of software and hardware, specifically breadboard implementations. An advantage our team will provide is a further and more detailed understanding of the i281 CPU architecture and develop lab work to benefit whoever wants to understand the i281 CPU. Another advantage is our CPU is unique and there is not as much, if anything, like it on the market.

4.1.3. Technical Complexity

Our project has many moving components and different labs that can utilize these components. The labs consist of a mix of hardware and software labs that cover the various components related to computer architecture, like the ALU, program counter and seven segment display, along with the opportunity to troubleshoot and debug hardware issues of these labs and components. From a design standpoint, our project is made from an educational perspective and one of the many challenges is gauging the level of difficulty of each lab for a variety of audiences ranging from middle school to highschoolers for outreach events, and university students for the CprE 3710x course.

4.2. DESIGN EXPLORATION

4.2.1. Design Decisions

For the first semester, we are focusing on completing four labs. The intro lab which will require a custom circuit to introduce students to breadboards, wiring, and standardizations. The MUX and Program Counter (PC) labs which will implement components used in the actual i281 CPU. Last, we plan to program an EEPROM which will be the first of two EEPROM labs. The second will use the EEPROMs to program a 7-segment display.

The first decision we made was which labs to implement in the first semester. We needed to familiarize ourselves with the CPU so starting with the MUX and PC were easy starting points. In building these on breadboards, especially the PC, we came up with new layouts that will ideally have cleaner wiring for students to more easily build.

In ordering parts, we discovered that the EEPROM (W27C512), used in the existing design, is no longer in production. We came up with a replacement that would meet as many specs as possible and decided on the AT28C64B-15PU which has less storage but is cheaper and maintains an adequate speed unlike other replacement options.

We also came up with a timeline for all ten labs. The first few labs are very hardware-oriented, but the CPU has its own set of assembly instructions, so we needed to make sure to incorporate that. We decided on one of the later labs to implement rock, paper, scissors on the CPU where the inputs will be pushbuttons for each user and a series of LEDs or 7-segment displays.

4.2.2. Ideation

When deciding what labs to do, each of us came up with two ideas. This included an introductory lab, visualizing flip flops, rock paper scissors, memory storage on breadboards, tic tac toe, a maze using joysticks, and nim. Based on these options, we further fleshed out what labs Professor Stoychev had in mind and prioritized the labs based on that. This introduced us to the idea of a couple EEPROM labs. We then decided a good, interactive lab would be rock paper scissors which would be more software heavy to offset the first labs. It can also be visualized using the work done in previous labs including the EEPROM 7-segment display code. With that game in mind, we had most of our labs filled up and planned to continue further fleshing them out.

4.2.3. Decision-Making and Trade-Off

After discussing our lab timeline with the client, it became clear that most of the labs were already scoped out including the introduction lab, a MUX, PC, and ALU labs, two EEPROM labs, device drivers, and a final project. This left us with two labs of our choice including a game, which Professor Stoychev had suggested in the proposal, for which we decided on the rock paper scissors game since it will be straightforward to represent on the CPU and can incorporate the previous 7-segment display lab.

4.3. PROPOSED DESIGN

4.3.1. Overview

Our project consists of implementing 10 interactive labs. It combines material from some of the core computer engineering classes, CprE 2810, CprE 2880, and CprE 3810, and helps students associate the material with physical implementations. The key components of our projects are our circuits, diagrams and lab manual for each activity.

Description of each class:

- 2810: Introduction to digital logic consisting of digital logic gates, making more complicated circuits like flip flops, counters and registers
- 2880: Embedded systems; programming drivers
- 3810: Implementing a RISC-V processor in Verilog which is based off CprE 2810

Each class has a concept implemented in one of the 10 labs. For example, the current working labs are related to mainly 281,381, and a small bit of 288 on the hardware end. The labs that relate to 281 are chips and breadboards, MUX, PC and rock paper scissors lab. The labs that relate to 381 is the ALU lab. The KiCad and EEPROM labs relate to the CprE 2880 class.

4.3.2. Detailed Design and Visuals

The key components of our projects are our circuits, diagrams and lab manual. Our labs consist of the following sections:

- Prelab: Questions for students to answer to place a baseline expected knowledge before they start the lab.
- Objectives: The purpose of this lab.
- Background: This is also related to the prelab, which is what kind of components and concepts will be used in this lab.
- Standardization and Implementation: How this lab will be expected to be implemented and evaluated for the teaching assistants.
- Activity for lab: A description of which topic the class is currently studying to help students understand the material of this class a bit more. Also, a problem statement for what they need to do and which documents and hints they can refer to.
- Steps and Results: Details of the steps needed to complete this lab whether they are calculations, word or picture descriptions. In addition, what the expected outputs would be for the labs.

4.3.3. Functionality

Our design will operate as a series of labs attached to an experimental class that students who are interested in computer engineering can use to attain a better understanding for the previous classes they took if they were to be a college student at Iowa State University. For other students who are not familiar with this, the labs can serve as a basic understanding of computer engineering overall.

4.3.4. Areas of Concern and Development

There are different levels of user satisfaction:

- Basic: A very rough lab draft, testing circuit works, circuit or lab works mostly (70%-80%)
- Moderate: A revised lab draft that may need more iterations, testing circuit works, circuit or lab works mostly (90%-95%)
- Excellent: A revised lab that went through many iterations, testing circuit works, circuit or lab works completely

Primary concerns: Lab draft may not be clear enough for TAs and the professor. In addition, we are concerned that our team may not be able to gauge the success rate of students, as in, the students may find it too difficult to complete the lab, resulting in discouragement.

Questions to professor and TA(s):

What can be considered as a successful lab?

What can our project do to help the students enjoy the lab material but also not overwhelm them with it?

What kind of instructions can we improve to give the students and TAs to help them understand/instruct the lab?

4.4. TECHNOLOGY CONSIDERATIONS

The first main technology used in our design are breadboard circuits. The advantage of using breadboards is that they are very easy to test circuits and designs in an inexpensive and quick way. This allows us to make changes to the original circuit designed for the i281e processor. This also allows us to prototype what we are asking the students in our design to do where we can get an idea for how long a circuit takes to build on a breadboard. The main weaknesses of breadboards is that parts are not soldered in and thus have a tendency to come loose if not handled with care. In addition, parts placed in a breadboard are generally more fragile because of their cheapness and parts can become damaged without an easy way of testing them out. In addition, breadboards themselves can break from time to time and cause issues that way. But we decided to go with breadboards anyway because they provide them with the most accessibility to physically building circuits.

The second technology we are using in our design is KiCad. KiCad allows us to design circuits that could later be printed onto PCBs. The main advantage of using KiCad is that the previous team's designs were made in KiCad so no translation of circuits into a different program needs to be done. In addition, it makes it very easy to see what values of the chip's inputs are and which are outputs. Some weaknesses of KiCad is you can't make the diagram follow which side the pins are on so, in KiCad all inputs are to the left and all outputs to the right. This makes it difficult to visualize how the circuit will look on a breadboard because of this. In addition, the images produced from KiCad are not easy to read the small numbers so sometimes it takes some educated guessing to figure out which pin the diagram meant. Overall, we went with KiCad because of its previous use on the team and possible future lab portions will use KiCad to show PCB design.

The final technology we have used in our design is TinkerCad. TinkerCad is a website that allows us to generate clean images of the breadboard circuit so that wiring that may obstruct the view for those just following the pictures have a clear view on where the circuits connect. As mentioned before the strength of TinkerCad is its clarity in circuit wiring compared to just an image of the circuit. A weakness of TinkerCad is that it doesn't have all the chip layouts we need but we spent some time and custom made them. Overall TinkerCad was chosen because it generates those very clear images that makes the labs as easy to follow as possible.

4.5. DESIGN ANALYSIS

As previously mentioned, we create our lab in stages. These stages are designing the lab, ordering parts for the lab, building the hardware or code the software to mockup the activity for the lab, testing the design for the lab, then finally documenting. Currently, we have Lab 6, the program counter, in the documentation stage. We have Lab 8, the 7-segment decoder using an EEPROM, in the testing stage. And Lab 1, implementing digital logic, along with Lab 3, the bus MUX, are completed.

As it stands our design is currently working as we have not had to scrap a lab yet. We have been able to implement multiple circuits and have a lab that is almost complete. Thus, while we have not tested with any TA's or students our labs seem feasible. But as we only have one lab at the moderate stage of development with three still at the basic stage it's still too early to tell if all our lab topics are plausible. Once we implement more of the labs, we'll be able to decide how to better structure our labs timeline.

For our future state we plan on finishing the labs currently in progress and beginning more labs. This includes more design, implementation and testing with the new labs. As our project is a curriculum of labs, we also plan on further designing the progression of the labs, additional testing materials, such as test circuits or programs, and any additional circuits, programs or interfaces that we find the need to create. Given the promising start with the MUX lab, we believe that we will be able to complete the rest of the labs. Our only hurdle is making sure that we can secure the necessary materials as needed.

5. Testing

5.1. UNIT TESTING

For each of our breadboards our main methods of testing include multimeter voltage testing and unit testing with our test board. With multimeter testing we can probe voltages at different points in the circuit to allow for us to check if a component is working as expected.

In addition to multimeter testing, we also test circuits used in labs with a test board. Our test board consists of

- 2 sets of 8-switch dip switches which allow us to provide two 8-bit inputs.
- 3 sets of 2-switch DIP switches which allows for up to 6 various select lines.
- 2 debounced push buttons which allows for a manual clock input.
- 8 LEDs used to display the output of the circuit.

There are plans for next semester to create a PCB of this test board, see figure 2, usable in labs to allow for a sturdier implementation that can stand up to more rough use in a lab setting where a student would just need to plug in their design to the board without having to worry about pin placement.

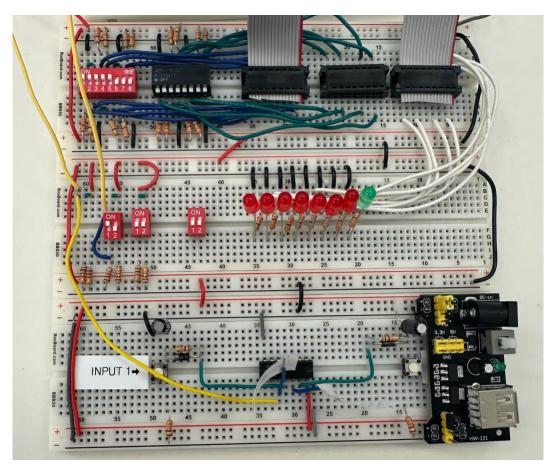


Figure 2 - Breadboard Mockup of Test board Connected to PC Circuit

5.2. INTERFACE TESTING

The main way of interfacing with our designs is through our labs and through our test board described above in unit testing. The labs are how we are demonstrating our design ability and testing the labs was done through a rigorous editing process and testing with students who may take the class. Future testing may include testing with the board itself. With the testing board we are able to test if the breadboard units designed will interface properly with the i281e processor which is a good way to show that the designs we have created properly interface with the processor.

5.3. INTEGRATION TESTING

The main process of integration testing is ensuring that all the lab materials, components, activities and instructions all function together to achieve the lab's goals. The most critical path is the integration of the breadboard design to instructions. It's important for instructions to be clear and unambiguous so that the lab can be followed and completed within the requirements. This can be tested with rough drafts of labs and run throughs with students to ensure that all the information is being correctly translated to the lab.

5.4. SYSTEM TESTING

For our system testing we are using students around the experience of those who will be doing the labs and having them do the activities and see where improvements or clarifications can be added to the activities and directions. In doing this we are not only getting feedback on the labs from those who would be doing it but ensuring that the labs are of appropriate length and difficulty to fit without our requirements.

5.5. REGRESSION TESTING

We ensure that new labs and breadboard don't break old functionality by following a strict set of standardization when it comes to interfacing between components and following a set guideline when creating labs to make sure that even if different people worked on the same part of a lab that a student wouldn't be able to tell. Most of these standards we are following were laid out by the previous i281e senior design groups.

5.6. ACCEPTANCE TESTING

In the creation of circuits and labs whenever we have a mockup or a draft, we involve the client by having him go over our designs or drafts and leave feedback. With the circuits this mainly involves checking if the placement of the components make sense, if standards are being followed and if the circuit is clean enough to be understood. In terms of the labs our client and us work together in red pen to make changes that the client wants to the lab whether it be adding more sections or making edits. This ensures that the quality of the product is where the client wants it and that all requirements are being met.

5.7. RESULTS

Through one of the tests, we did with a student they were able to complete our MUX lab in 1 hour and 46 min with help from one of our group members who acted like a TA/group partner to them. This

demonstrated that we were falling short of the 2-hour mark of a lab but with setup and cleanup can meet that 2-hour requirement. This helped us clean up some of the wording in our activity for the MUX and get a real timeline on how long an activity like this will take. Our next steps will be to repeat testing with similar students to get a wider range of results and feedback. This will allow us to have the best final product going forward.

6. Implementation

6.1. IMPLEMENTATION PROCESS

For our implementation process we are approaching our labs one at a time. First we select and design a lab from our designed curriculum. Then we order the parts needed to implement any hardware components for the lab. Once the parts arrive, we begin implementing our designed activity for the lab. For implementation we work through the activity that the students will be completing in the lab and build any testing components or programs needed. This lets us gauge roughly how long the activity will take to complete. It also informs us of potential challenges students may face if we make the lab according to our initial design.

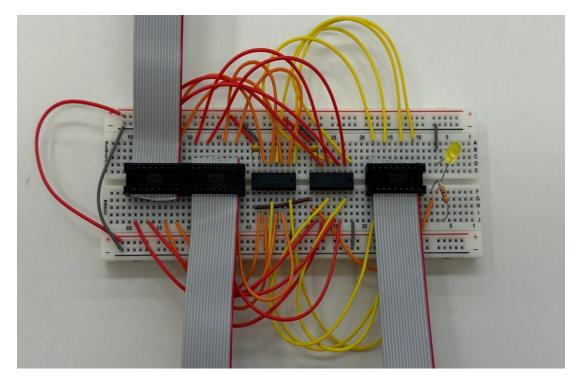


Figure 3 - Initial Implementation Lab 3's 2-to-1 8-bit Bus Multiplexer

While we work through the activities, we closely monitor any difficulties that we face in completing the activity. Difficulties include unusual results when testing components, problems with IDEs or design programs, designs that do not give us accurate results and things we learn by going through the activity that are helpful for completing it. If the designed activity has any major problems or it does not give us the intended results, we adjust the design to remedy the problems. Once a design is thoroughly tested and all the major and a majority of the minor problems are worked out. We bring the lab before the team and client for approval. Once a lab has been thoroughly tested and approved by both the team and client we begin drafting the first draft of the lab documentation.

6.2. DRAFTING LABS

Each lab features two main and additional supporting documents. The two main documents are the lab manual and the lab report. While supporting documents range from grading rubrics and answer keys to specification sheets and supplemental resources.

Each lab manual features five main sections.

- Lab Objective
- Background
- Activity
- Testing
- Parts List

The contents of the lab reports change depending on the content of the lab. The only part that will always be present is the prelab.

Once the first draft is finished the team consults the client for feedback. After receiving feedback the team makes required, clarifying and formatting changes necessary to the lab. Then the process is repeated until both the team and client are satisfied with the lab.

CprE 3710x Lab X Electrical and Computer Engineering Iowa State University

1.0 Objectives

What do we want to accomplish with this lab? What should the students get out of the lab? What does this lab cover?

2.0 Background

What information do the students need to understand before working through the lab? Does this lab require any logic? How does the circuit work? What will the student's find difficult to figure out if it's not included? Subsections might be dedicated to different parts of the lab or included prior to the activity step where the information is needed.

3.0 Activity

What steps do the students need to do to complete the lab? This is where the points are, what do the students need to accomplish to get these points? Offer general guidance, but how much direction is necessary for a student to draw the necessary conclusion on how to complete the activity?

3.1 Specific Activity Step

What is the first step to the overall goal of this lab?

Figure 4 - Beginning of Lab Manual Template

6.3. CURRENT PROGRESS

As a team we have three labs in drafting, and another is in implementation. Our first lab has a finished lab report and a completed first draft.

CprE 3710x Lab 1 Electrical and Computer Engineering Iowa State University	Implement a 2-to-1 MUX
Name:	Student ID:

Lab Section:

Date:

Prelab

Complete the truth table for the following Boolean function: $f = sx_1 + sx_2$

s	<i>x</i> ₁	<i>x</i> ₂	\overline{sx}_1	sx ₂	f
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Figure 5 - First Section of Lab 1 Report Template

Lab three has the first draft of the lab report completed and the lab manual is in its fourth revision.



4.0 Activity

Students need to complete the pre-lab to help complete this lab. In addition, they need to understand which pins go where and the rotation of the chips.

4.1 Place the Bus Connectors and Chips

- The connectors should span pins 60-53, 50-43, and 20-13.
- -The Chips should span pins 40-33 and 30-33.
- Next, connect the source and ground lines on the top and bottom of the board and connect the chips to the source and ground as pictured below.

Before continuing to the next step, have your circuit checked by a TA.

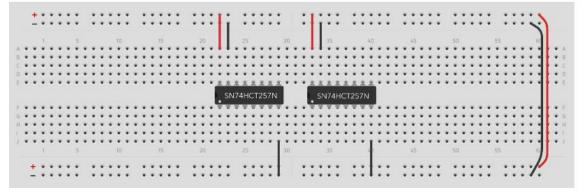


Figure 6 - Excerpt from Lab 3 Manual

Lab five has completed implementation and as the activity took more time than we expected we made it into a two-part lab. We are currently working on the first draft. Lab 7 began its implementation as the initial design was finished.

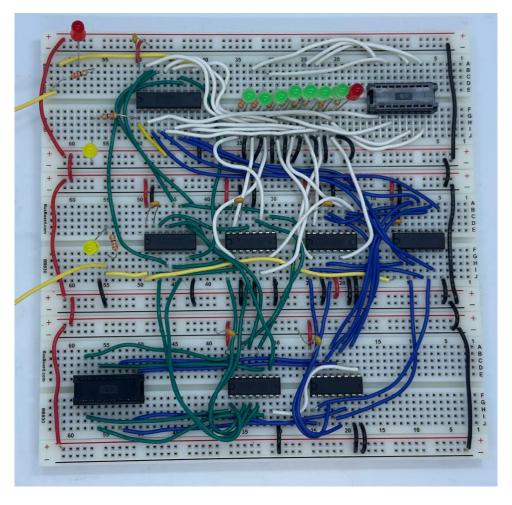


Figure 7 - Lab 5 & 6 Implementation

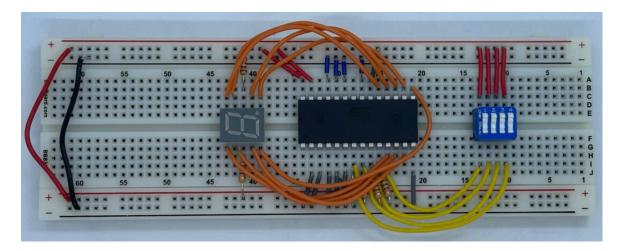


Figure 8 - Beginning of Lab 7 Implementation

7. Ethics and Professional Responsibility

This discussion is with respect to the paper titled "Contextualizing Professionalism in Capstone Projects Using the IDEALS Professional Responsibility Assessment".

7.1. AREAS OF PROFESSIONAL RESPONSIBILITY/CODES OF ETHICS

It's important that we effectively communicate design progress and feasibility to each other as well as the client. Based on this communication, we can further improve our labs and speed up our workflow. Our team upholds ethical standards since our project is an educational one, it is important to follow the IEEE code of ethics and the university's code of ethics by setting a good example for the students who will be taking this course. Our ethics for this project most likely lines up with Benjamin Franklin's virtues. Since, our project is for educational purposes and our team operates on honesty and integrity. In addition, our team is upfront about any potential issues that concerns the i281e processor.

Area of Responsibility	Communication Honesty
Definition	Reporting work, truthfully without any form of deception to advisors, professors or any faculty who is supervising the project. In addition, that includes truthfully reporting to the public.
Relevant Item from Code of Ethics	Our team reports truthful work with our project advisor and senior design advisors. If there is a concern in our project, our team would bring attention to that concern right away to find ways to address this issue as soon as possible.

Table 5 - Professional Area of Responsibility

7.2. FOUR PRINCIPLES

	Beneficence	Nonmaleficence	Respect for Autonomy	Justice
Public Health, Safety & Welfare	Students will gain experience and learn from our labs	Students will learn in a safe and well- guided environment by the TAs and professor	We must make sure students are able to gain experience rather than just following instructions	We need to make a fair grading standard
Global, Cultural & Social	People from different backgrounds and universities can use our open-source software	We need to make sure that our open- source software is safe to use	We need to make sure that our instructions of our open-source software are user-friendly and clear to read for all users	Making sure that our open-source software is not plagiarized
Environment al	What students learn in this course may enable some of them to leverage their careers positively later	We need to keep in mind that we are using a lot of plastic materials and not use more than needed	We need to make sure that our project does not harm the environment and find optimal methods for better use of our resources without also being wasteful	Make sure the materials we source is from a respectable company and not wasted
Economic	Students are going to have to pay for materials, we need to make sure what they learn is worth the cost	Make sure students don't pay more than necessary	Keep in mind the cost burden to the department and individual students	Make sure students pay for what they use

Table 6 - Four Principles

7.3. VIRTUES

Our team believes that communication honesty, financial responsibility and sustainability are important for many reasons. It is important to report honestly in a timely and professional manner since our attitude towards the project and faculty as a team reflects and may influence how students and participants in the labs treat the classwork and lab work. It is also important to our team to be financially responsible and sustainable since the project is also made for future students and individuals who are interested in replicating those labs.

Team Member	Ethan	Ariana	Tessa	Gigi
Virtue Demonstrated	Honesty	Clear and Through Documentation	Attentiveness	Commitment to Quality
Virtue Importance	It's important to be honest in reporting so that all team members are working with the same information and that what you say can be trusted to be true.	It's important to clearly and effectively communicate information when it's included in project documentation, so it can be understood by readers.	It's important to be responsive to the needs of teammates, the project, and the client and be able to prioritize them and come up with workable solutions to them.	It's important to have a quality documented lab, and that also means that it is important to have constructed lab work of the same quality to ensure that student(s) comprehend the information being given to them.
How was it Demonstrated?	Honest reporting of what was worked on and when.	Thoroughly creating documentation for the labs and editing group documentation.	Working with the client to improve several drafts of a lab and get it to a final state.	Going through detailed and thorough testing of our labs to make sure that the concepts are correctly implemented, along with updating lab documentation whenever there is a change in implementation method.
Virtue to Improve	Industry	Frugality	Cooperativeness	Completeness
Virtue Importance	It's important to make sure that little time is wasted in meetings and work sessions so those meetings can be as productive as possible.	It's important to make sure that components are not wasted to keep costs manageable. It's also important that components are used with care and not recklessly gone through.	It's important to be flexible and open to other teammates' ideas. After communicating our ideas, and those of the client, we need to resolve any creative differences.	It's important to make the lab reports feel more like they are made for an engineering course. It's also important to provide the full, detailed information about what the labs would entail and what the questions are really asking the students to do.

Team Member	Ethan	Ariana	Tessa	Gigi
How Can it be Improved?	Following the Ganntt chart much closer next semester to make sure all labs get done on time and not to fall behind on what is planned.	By being more careful when using components and not being reckless with materials.	Our ideas for some labs are not completely fleshed out and I sometimes focus too much on how I want the lab timeline to work.	It is important to go through many iterations of the lab documents and involve our advisor and other participants in outreach events to provide input about the instructions made in the labs.

Table 7 - Virtues and Improvements within the Team

In conclusion, our commitment to honest communication, financial responsibility, and sustainability not only enhances the integrity of our project but also sets a positive example for future students and participants. By incorporating these principles into our work, we aim to create a legacy that encourages responsible practices and fosters a culture of collaboration and respect within the academic community.

8. Closing Material

8.1. CONCLUSION

Our project's primary goal is to develop ten interactive labs to help students understand processor design and digital logic. These labs are designed to be completed within a 2- to 3-hour lab period and will be supported by comprehensive materials, including documentation, guides, and potential video tutorials. So far, significant progress has been made in developing these labs, with this first semester focusing on four labs: an introduction to breadboards, the bus MUX, the program counter, and an initial EEPROM lab. These labs provide hands-on experience with hardware and software components, helping students visualize how processor components interact. Other labs, such as an introduction to assembly-level programming and the rock-paper-scissors game, are also in the planning stages.

The project has a secondary goal of assembling and testing additional i281e processors (to the one built by a previous senior design team) and documenting that process for future students, TAs, and hobbyists. Finally, we have a stretch goal to offer outreach activities to middle and high school students to spark interest in computer engineering. We have some existing materials and have investigated these goals to scope them out, but plan to implement them next semester.

To achieve all these goals, we follow a structured approach that breaks down the project into milestones, each corresponding to a finalized lab. The development process is divided into research and prototyping, building and testing, and refining the lab documentation. The focus has initially been on hardware labs and will soon progress to software-focused labs and those that integrate both. Our team will gather continuous feedback from students and advisors to refine the labs and ensure they align with course material, clarity, and usability.

Several constraints have impacted the project's progress. Limited hardware resources and free software tools, which lack advanced features, have been challenges. Additionally, the labs must be designed to fit within a 2- to 3-hour timeframe, which has required tracking time and testing for feasibility. Procuring materials has presented challenges, particularly for more complex labs that require specific components such as EEPROMs and custom assembly programs.

For future iterations of the design and implementation, streamlining material procurement will be crucial to ensure that all necessary components are available on time. Testing methods can be enhanced by developing a more robust PCB version of the test board for use in the labs. Additionally, utilizing more advanced software tools for circuit design could help overcome the limitations of current free tools. Lastly, ongoing student feedback will refine lab manuals and instructions, ensuring that the labs remain clear, compelling, and engaging for students.

8.2. **R**EFERENCES

- A. Stoytchev, "CprE 281: Digital Logic (Fall 2023)," Dec, 2023. [Online]. Available: https://www.ece.iastate.edu/~alexs/classes/2023_Fall_281/. [Accessed Dec 6, 2024].
- B. Damman, "i281 CPU," May, 2024. [Online]. Available: https://github.com/brandtdamman/i281e-cpu. [Accessed Dec 6, 2024].
- [3] E. Mirecki, "7 Segment Controller via EEPROM," July, 2022. [Online].
 Available: https://elijah.mirecki.com/blog/7-segment-eeprom. [Accessed Dec. 6, 2024].
- "IEEE Recommended Practice for Electronic Power Subsystems: Parameter Definitions, Test Conditions, and Test Methods," in IEEE Std 1515-2000, vol., no., pp.1-84, 15 Sept. 2000, doi: 10.1109/IEEESTD.2000.91922.
- [5] "IEEE Standard Glossary of Computer Hardware Terminology," in IEEE Std 610.10-1994, vol., no., pp.i-, 1995, doi: 10.1109/IEEESTD.1995.79522.
- "IEEE Standard Glossary of Computer Languages," in IEEE Std 610.13-1993, vol., no., pp.i-, 1993, doi: 10.1109/IEEESTD.1993.119224.
- [7] "maze-game," June, 2022. [Online]. Available: https://github.com/cheblankenshipUTD/maze-game/commits/main/. [Accessed Dec 6, 2024].
- [8] sdmay24-14,"Team14 Final Presentation", ece.iastate.edu. Available: https://sdmay24 14.sd.ece.iastate.edu/final/2024/492_Team14_FinalPresentation.pdf [Accessed Dec 6, 2024]
- [9] sdmay21-38,"i281 Processor Simulator", ece.iastate.edu. Available: https://sdmay21-38.sd.ece.iastate.edu/docs/DDV1.pdf [Accessed Dec 6, 2024]
- [10] sdmay22-20, "Implementing the i281 CPU", ece.iastate.edu. Available: https://sddec22-20.sd.ece.iastate.edu/ [Accessed Dec 6, 2024]

8.3. APPENDICES

8.3.1. Research

8.3.1.	Research			
Product Services and Design	CprE 381 Lab 1 Documentation	Qatar University 261 Lab 2: Logic Circuits	Iowa State University CprE 288 Lab 5: Interrupts	CprE 281 Counters Lab Documentation
Unique Value Proposition	This lab is the first stage of CprE 381 which culminates in designing and building a MIPS processor. In this lab, students test the output of several provided components as well as design, build, and test a full adder and an N-bit adder.	This lab explores different ways of creating logic circuits using different logic chips (LC) and different ways of implementing the same design.	This lab is tailored to the Tiva TM4C123GH6PM Processor and requires knowledge of the processor's inner workings or the ability to read its documentation to complete. The purpose of this lab is to demonstrate how interrupts work within an embedded system.	This lab is about basic digital logic and builds up to gaining knowledge about how to combine certain logic gates to create efficient components.
Product Advantages	All the components designed and tested in this lab are subcomponents of the processor students will put together later so this helps students understand each component for later.	This product includes pin diagrams and helpful pictures to follow step-by-step instructions while exploring the basic concepts of logic circuits.	This lab provides skeleton code and resources so that to complete it a student would only have to mess with the relevant parts of the code while understanding the concepts presented in the lab.	This lab provides a basic understanding of how a part of our product works and our team could tweak the code if we wanted to, instead of having to build it from the ground up.
Product Disadvantag es	There are not a ton of instructions on getting started or steps to follow throughout the lab making certain questions misleading or confusing to understand.	This lab requires the ability to read circuit diagrams although the pictures can help circumvent the need to read these diagrams.	This lab requires extended readings and prior knowledge not included in the documentation to complete. There is a learning hurdle in understanding how to read microcontroller documentation.	The lab may require knowledge about what flip flops and clock speeds are. In addition, this lab requires knowledge of how each flip flop is different when connected or disconnected.
User Pros	Gives them a chance to understand the individual components and start designing some as well.	Easy to understand and follow. All the information is contained within the lab. Gives helpful tips to stay organized while building the design.	The concepts are easy to understand and implement if you can read the datasheet and pay attention to class.	The concept is easy to understand with enough practice and does not require complex calculations.

User Cons	This lab is very time consuming and makes it difficult to understand where to start.	The whole lab takes a lot of time to complete if the time isn't taken previously to fill out some of the diagrams and truth tables.	The lab is time consuming and takes a lot of time outside of the lab to complete. The provided equipment occasionally glitches and doesn't work as it is supposed to. If you don't understand the datasheet it's really challenging to complete.	The lab may require a truth table that is accurate, meaning that the user needs to track each input and output of the counter and the flip-flops contained in the counter's circuit.
-----------	--	--	---	---

Table 8 - Product Research

9. Team

9.1. TEAM MEMBERS

- Ethan Uhrich
- Ariana Dirksen
- Tessa Morgan
- <u>Gigi Harrabi</u>

9.2. REQUIRED SKILL SETS FOR YOUR PROJECT

Skill Set	Rationale
Circuit building	The first set of labs we are creating require skills to build and modify breadboard circuits based off of previous KiCad Designs.
Detailed writing and editing	In the creation of labs it is important to create detailed and understandable directions for students and others to be able to follow along with.
Photo editing and image generation	It's important for labs to be visually appealing so having engaging but professional images to go along with our labs.
EEPROM programing	One of the labs in progress is EEPROM programming which the i281e processor uses for its main and code memory.
Circuit testing	In addition to circuit building it's important to know how to test if a circuit is functioning as intended and troubleshooting steps involved with fixing a circuit.
Digital logic	Most of our labs are centered around digital logic so it's important to have the knowledge to write labs around it.
KiCad	Most of the designs left by the previous team were made in KiCad. We had to learn how to read these designs and how to edit and implement them onto breadboards.

Table 9 - Skills Needed for the Project

9.3. SKILL SETS COVERED BY THE TEAM

Skill	Team Member
Circuit Building	Ariana, Ethan, Tessa, Gigi
Detailed writing and editing	Ariana, Ethan, Tessa, Gigi
Photo editing and image generation	Ariana, Tessa
EEPROM programing	Tessa, Gigi
Circuit testing	Ethan, Ariana
Digital logic	Ariana, Ethan, Tessa, Gigi
KiCad	Tessa, Ethan

Table 10 - Skills Covered by the Team

9.4. PROJECT MANAGEMENT STYLE ADOPTED BY THE TEAM

As a team we are operating under Agile project management style as our process for creating the labs requires us to revise our designs and the labs multiple times before they will be ready. Throughout our planning and implementation processes, we have already scrapped multiple lab ideas, so we've been using Agile to adapt to changes as they appear. It's also imperative that we're able to jump from one task to the next whenever one is stalled to make sure that we are still working on our project. The stand-ups involved in the agile project management style also allows us time to communicate on what everyone is working on and will be working on through the week and gives time to talk about any challenges we are facing in our own assignments.

9.5. INITIAL PROJECT MANAGEMENT ROLES

- Ethan Uhrich Treasurer, Team Lead
- Ariana Dirksen Note Taker, Editor
- Tessa Morgan Task Manager, Webmaster
- Gigi Harrabi Client Interaction, Outreach Coordinator

9.6. TEAM CONTRACT

Team Name sdmay25-31

Team Members:

1) Ethan Uhrich	2) Ariana Dirksen
3) <u>Gigi Harrabi</u>	4) <u>Tessa Morgan</u>

Team Procedures

- 1. Day, time, and location (face-to-face or virtual) for regular team meetings:
 - a. Thursday, 2:15pm Coover 1301 Team Meeting
 - b. Monday 10-11am Durham 303 Advisor/Client Meeting
 - c. Wednesday 11am Coover 1301- Optional Additional Team Meeting
- 2. Preferred method of communication updates, reminders, issues, and scheduling (e.g., e-mail, phone, app, face-to-face):
 - a. Discord
 - b. E-mail Outside of team correspondence
- 3. Decision-making policy (e.g., consensus, majority vote):
 - a. Majority vote if disagreement. If tied, the Advisor/Client is the tie-breaker.
- 4. Procedures for record keeping (i.e., who will keep meeting minutes, how will minutes be shared/archived):
 - a. Ariana will keep notes stored in a Folder in shared Google Drive.

Participation Expectations

- 1. Expected individual attendance, punctuality, and participation at all team meetings:
 - a. Attendance is expected but exceptions will be made with notice.
 - b. Punctuality: Be on time if not early. If running late, notify the group via discord.
- 2. Expected level of responsibility for fulfilling team assignments, timelines, and deadlines:
 - a. Get things in on time, if not early.
 - b. Ask for help early, not at the last minute.
 - c. Communicate with the team if you will miss a deadline.
- 3. Expected level of communication with other team members:
 - a. Emote to important messages that don't require a text response.
 - b. Respond to important messages within a day
- 4. Expected level of commitment to team decisions and tasks:
 - a. Decisions should be promptly decided on
 - b. Tasks need to be done by deadline, but MUST be completed by drop-deadline.
 - c. If subtask is needed by another team member due by deadline, finish in time for deadline.

Leadership

- 1. Leadership roles for each team member (e.g., team organization, client interaction, individual component design, testing, etc.):
 - a. Ethan Uhrich Treasurer, Team Lead
 - b. Ariana Dirksen Note Taker, Editor
 - c. Tessa Morgan Task Manager, Webmaster
 - d. Gigi Harrabi Client Interaction, Outreach Coordinator
- 2. Strategies for supporting and guiding the work of all team members:
 - a. Routine checks during weekly meetings (weekly standup)
- 3. Strategies for recognizing the contributions of all team members:
 - a. Kudos, physically represented with Gold Star Stickers
 - b. Personal and team affirmations

Collaboration and Inclusion

- 1. Describe the skills, expertise, and unique perspectives each team member brings to the team.
 - a. Ethan Only Male, Lots of team-leading experience.
 - b. Ariana Tutoring experience, Ran a high school science club.
 - c. Tessa Taught in "Girls Who Code", CprE 185 TA
 - d. Gigi Experience with academic correspondence
- 2. Strategies for encouraging and supporting contributions and ideas from all team members:
 - a. Weekly Stand-ups
 - b. Round Robin
- 3. Procedures for identifying and resolving collaboration or inclusion issues (e.g., how will a team member inform the team that the team environment is obstructing their opportunity or ability to contribute?)
 - a. Go to an advisor with systemic problems.
 - b. Try to resolve smaller problems as a group.

Goal-Setting, Planning, and Execution

- 1. Team goals for this semester:
 - a. Create 3 of the labs/activities w/ documentation, videos
 - b. Do at least 1 outreach event
 - c. Outline the last 7 activities.
- Strategies for planning and assigning individual and team work:
 a. Tessa will assign tasks via git.
- 3. Strategies for keeping on task:
 - a. Standups, team lead making sure we don't go too far off topic during meetings/stand-ups

Consequences for Not Adhering to Team Contract

- 1. How will you handle infractions of any of the obligations of this team contract?
 - a. Gold stars revoked.
 - b. 3 strike system 2 warnings on 3rd escalate
- 2. What will your team do if the infractions continue?
 - a. After 3 strikes the issue will be escalated to the advisor.

a) I participated in formulating the standards, roles, and procedures as stated in this contract.

b) I understand that I am obligated to abide by these terms and conditions.c) I understand that if I do not abide by these terms and conditions, I will suffer the

consequences as stated in this contract.

1) 9/12/24 DATE 2) DATE 9/12/24 3) DATE 9/12/24 4) DATE 9/12/24